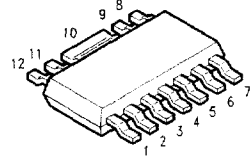


Preliminary Datasheet

- * Power amplifier for GSM or AMPS application
- * Fully integrated 2 stage amplifier
- * Operating voltage range: 2.7 to 6 V
- * 2 W output power at 3.6 V
- * Overall power added efficiency 46 %
- * Input matched to 50 Ω, simple output match



ESD: Electrostatic discharge sensitive device, observe handling precautions!

Type	Marking	Ordering code (taped)	Package 1)
CGY 94	CGY 94	Q68000-A9124	MW 12

Maximum ratings

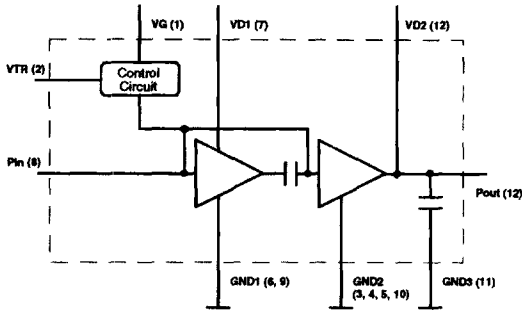
Characteristics	Symbol	max. Value	Unit
Positive supply voltage	V_D	9	V
Negative supply voltage ²⁾	V_G	-8	V
Supply current	I_D	2	A
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	-55...+150	°C
Pulse peak power dissipation duty cycle 12.5%, $t_{on}=0.577ms$	P_{Pulse}	9	W
Total power dissipation ($T_s \leq 81 \text{ °C}$) <i>T_s: Temperature at soldering point</i>	P_{tot}	5	W

Thermal Resistance

Channel-soldering point	R_{thChS}	≤14	KW
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1) Plastic body identical to SOT 223, dimensions see chapter Package Outlines
 2) $V_G = -8V$ only in combination with $V_{IR} = 0V$; $V_G = -6V$ while $V_{IR} \neq 0V$

Functional block diagram:



Control circuit:

The drain current I_D of the CGY 94 is adjusted by the internal control circuit. Therefore a negative voltage (-4V...-6V) has to be supplied at VG. For transmit operation VTR must be set to 0V. During receive operation VTR should be dis-connected (shut off mode).

Pin #	Configuration
1	VG Negative voltage at control circuit (-4V...-6V)
2	VTR Control voltage for transmit mode (0V) or receive mode (open)
3,4,5,10	GND 2 RF and DC ground of the 2nd stage
6,9	GND 1 RF and DC ground of the 1st stage
7	VD1 Positive drain voltage of the 1st stage
8	RFin RF input power
11	GND 3 Ground for internal output matching
12	VD2, RFout Positive drain voltage of the 2nd stage, RF output power

DC characteristics

Characteristics	Symbol	Conditions	min	typ	max	Unit
Drain current stage 1	$IDSS1$	VD=3V, VG=0V, VTR n.c.	0.6	0.9	1.3	A
	$IDSS2$		2.7	4.1	5.9	A
Drain current with active current control	ID	VD=3V, VG=-4V, VTR=0V	-	1.1	-	A
Transconductance (stage 1 and 2)	$gfs1$	VD=3V, ID=350mA	0.25	0.32	-	S
	$gfs2$	VD=3V, ID=700mA	1.1	1.3	-	S
Pinch off voltage	Vp	VD=3V, ID<500µA (all stages)	-3.8	-2.8	-1.8	V

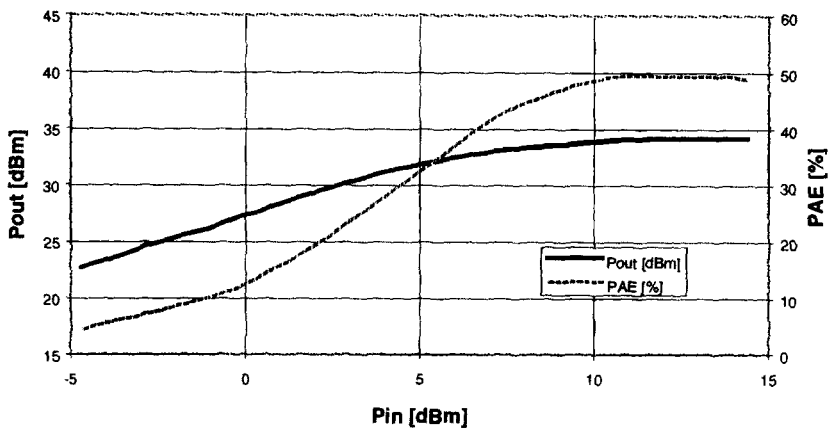
Electrical characteristics

($T_A = 25^\circ\text{C}$, $f = 0.9\text{ GHz}$, $Z_S = Z_L = 50\text{ Ohm}$, $V_D = 3.6\text{V}$, $V_G = -4\text{V}$, VTR pin connected to ground, unless otherwise specified; pulsed with a duty cycle of 10%, $t_{on} = 0.33\text{ms}$)

Characteristics	Symbol	min	typ	max	Unit
Supply current $V_D = 3.0\text{V}$; $P_{in} = 10\text{dBm}$	I_{DD}	-	1.18	-	A
Negative supply current (normal operation)	I_G	-	2	-	mA
Shut-off current VTR n.c.	I_D	-	400	-	μA
Negative supply current (shut off mode, VTR pin n.c.)	I_G	-	10	-	μA
Gain $P_{in} = -5\text{dBm}$	G	27.0	29.0	-	dB
Power gain $V_D = 3.6\text{V}$; $P_{in} = 10\text{dBm}$	G	22.8	23.6	-	dB
Output Power $V_D = 3.0\text{V}$; $P_{in} = 10\text{dBm}$	P_O	31.5	32.3	-	dBm
Output Power $V_D = 3.6\text{V}$; $P_{in} = 10\text{dBm}$	P_O	32.8	33.6	-	dBm
Output Power $V_D = 5\text{V}$; $P_{in} = 10\text{dBm}$	P_O	34.5	35.5	-	dBm
Overall Power added Efficiency $V_D = 3.0\text{V}$; $P_{in} = 10\text{dBm}$	η	43	48	-	%
Overall Power added Efficiency $V_D = 3.6\text{V}$; $P_{in} = 10\text{dBm}$	η	42	47	-	%
Overall Power added Efficiency $V_D = 5\text{V}$; $P_{in} = 10\text{dBm}$	η	41	46	-	%
Harmonics ($P_{in} = 10\text{dBm}$, CW)	$2f_0$	-	-	-49	dBc
$V_D = 3.6\text{V}$; ($P_{OUT} = 33.1\text{dBm}$)	$3f_0$	-	-	-45	dBc
Input VSWR $V_D = 3.6\text{V}$;	-	-	1.5 : 1	2.0 : 1	-

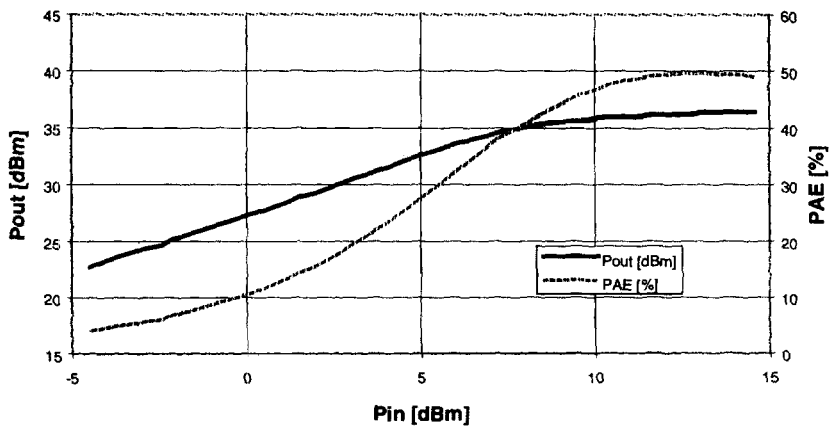
Pout and PAE vs. Pin

(VD=3.6V, VG=-4V, VTR=0V, f=900GHz, pulsed with a duty cycle of 10%, ton=0.33ms)

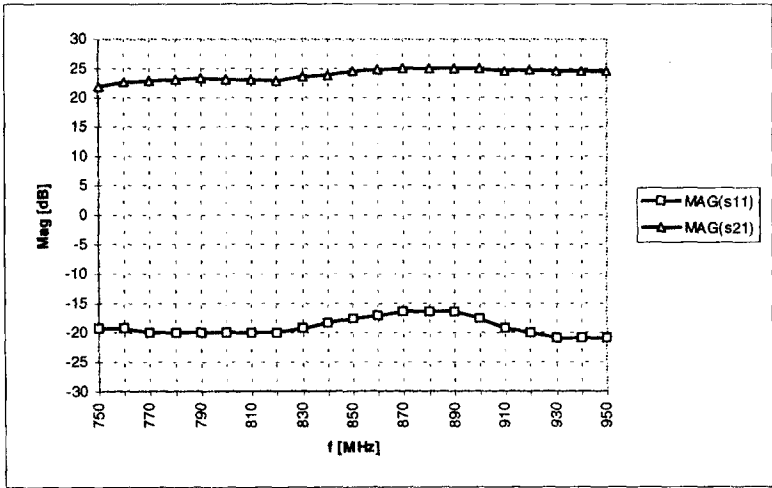


Pout and PAE vs. Pin

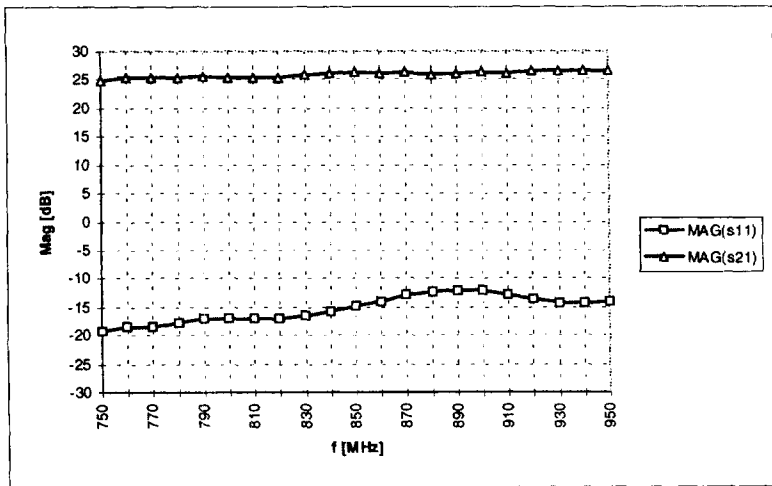
(VD=5V, VG=-4V, VTR=0V, f=900GHz, pulsed with a duty cycle of 10%, ton=0.33ms)



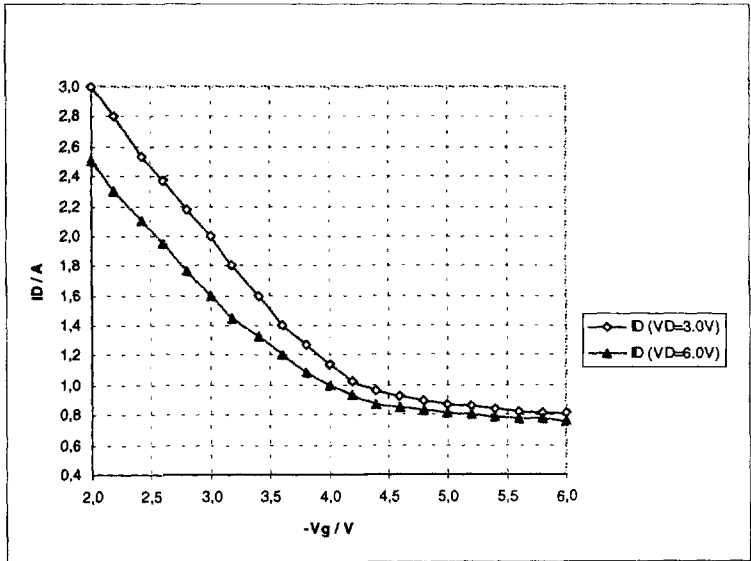
S-Parameter at VD=3.6V and Pin=9dBm
(VG=-4V, VTR=0V, pulsed with a duty cycle of 10%)



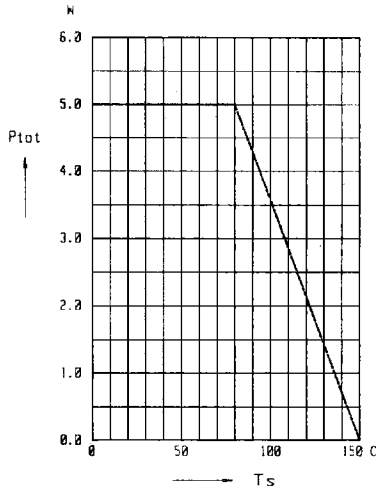
S-Parameter at VD=5V and Pin=9dBm
(VG=-4V, VTR=0V, pulsed with a duty cycle of 10%)



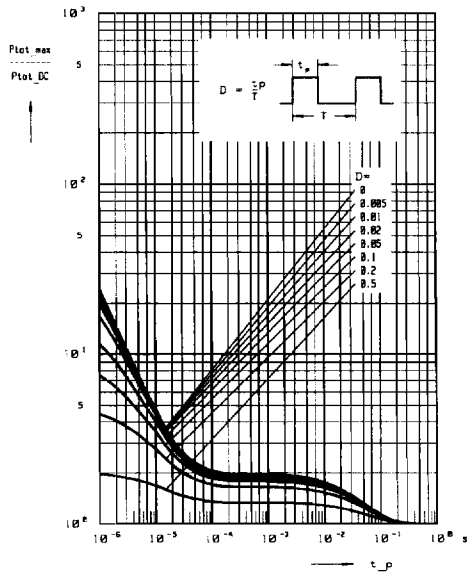
Performance of internal bias control circuit
($V_{TR}=0V$)



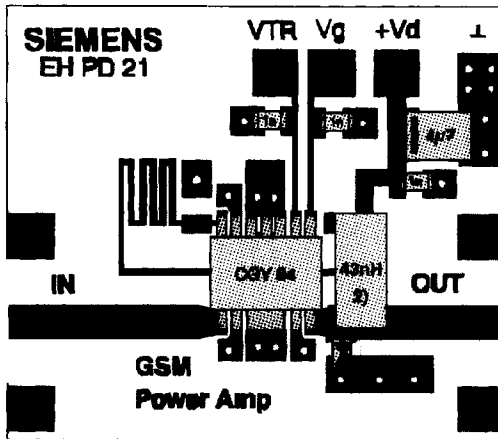
Total Power Dissipation $P_{tot}=f(T_s)$



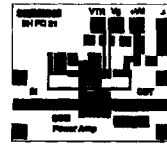
Permissible pulse load $P_{tot_max}/P_{tot_DC} = f(t_p)$



Test circuit board:



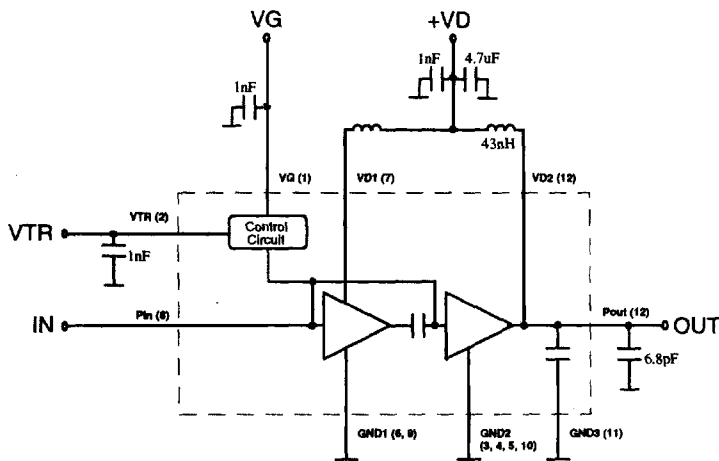
the CGY94 device (2-5mm).



Note:

By changing the position of the 6.8 pF capacitor at pin # 12 it is possible to tune the board for max. Pout or max. PAE. To achieve the maximum output power place the capacitor close to the CGY94. For a better PAE increase the distance between the capacitor and

Principal circuit:



- 2) Coilcraft SMD Spring Inductor
distribution by Ginsbury Electronic GmbH, Am Moosfeld 85 D-81829 München, Tel. 089/45170-223

APPLICATION - HINTS

1. CW - capability of the CGY94

Proving the possibility of CW - operation there must be known the total power dissipation of the device. This value can be found as a function of the temperature in the datasheet (page 7). The CGY94 has a maximum total power dissipation of $P_{tot} = 5 \text{ W}$.

As an example we take the operating point with a drain voltage $V_D = 3 \text{ V}$ and a typical drain current of $I_D = 1.0 \text{ A}$. So the maximum DC - power can be calculated to:

$$P_{DC} = V_D \cdot I_D = 3W$$

This value is smaller than 5 W and CW - operation is possible.

By decoupling RF power out of the CGY94 the power dissipation of the device can be further reduced. Assuming a power added efficiency (PAE) of 40 % the total power dissipation P_{tot} can be calculated using the following formula:

$$P_{tot} = P_{DC}(1 - PAE) = 3W(1 - 0.40) = 1.8W$$

2. Operation without using the internal current control

If you don't want to use the internal current control, it is recommended to connect the negative supply voltage at pin 1 (V_{TR}) instead of pin 2 (V_G). In that case V_G is not connected.

3. Biasing and use considerations

Biasing should be timed in such a way, that the gate voltage (V_G) is always applied before the drain voltage (V_D), and when returning to the standby mode, the drain voltage has to be removed before the gate voltage.